Product Design Specifications Data Sheet (PDS)
November 1999

(Pat. US 6,813,742 and US 6,799,295)

3GPP Turbo Codes Codec for Wireless Communications

1 Features

- Parallel Recursive Systematic Convolutional (RSC) Encoder as compliance with 3GPP Standards.
- Code rate 1/3, with K=3, and Trellis termination.
- Implemented Soft-in/Soft-out Log-MAP Decoders as compliance with 3GPP Standards.
- 3GPP Interleaver with Multi-stage interleaving.
- UMTS applications.
- Up to 50Mbps in ASIC, and 20Mbps FPGA block decoding
- Decoding up to 2 Mbps throughput for 3G W-CDMA, 3G CDMA2000 Wireless Communications.
- VHDL/Verilog Core solutions with IP license.
- Low power ASIC solutions.

VHDL Core Technologies

The Turbo Codes Decoder is designed and implemented in VHDL/Verilog source codes and can be synthesized for custom ASIC or FPGA technologies.

Applications

- UMTS, 3G W-CDMA, 3G CDMA2000 Wireless Communications.
- Wireless LAN and Wireless Local Loop.
- Satellite Communications, Cable Modem, HDTV, Digital TV.

2 Description

The 3GPP Turbo Codes Codec (Encoder/Decoder) is a patented Baseband Processor (Pat. US 6,813,742 and US 6,799,295) designed in compliance with the 3GPP Standards for 3G W-CDMA, 3G CDMA2000 and the UMTS wireless communications.

The 3GPP Turbo Codes Codec comprises of a Turbo Codes Encoder and a Turbo Codes Decoder. The Turbo Codes Encoder employs two (2) Recursive Systematic Convolutional (RSC) Encoder with Coding rate 1/3, Constraint length = 3, connected in parallel with an Interleaver preceding the second RSC encoder. The Turbo Codes Decoder employs two concatenated Log-MAP deocders with Forward and Backward computations, and Interleaver and Deinterleaver RAM buffers.

ICOMM's patented Turbo Codes Decoder is the most powerful forward error correction (FEC) commercially available today, operating near the Shannon limit and achieving greater power efficiency than current commercially available FEC schemes. As part of the patented Wireless Baseband Processor implements Turbo Codes Decoders with Diversity processing for computing signals from separate antennas, decoding multipath signals that have arrived at the terminal via different routes after being reflected from buildings, trees, or hills, which increases SNR by more than 6dB enabling data rates up to 2Mbps.

The device is packaged in TQFP, LGA, BGA.

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3 Pin Information

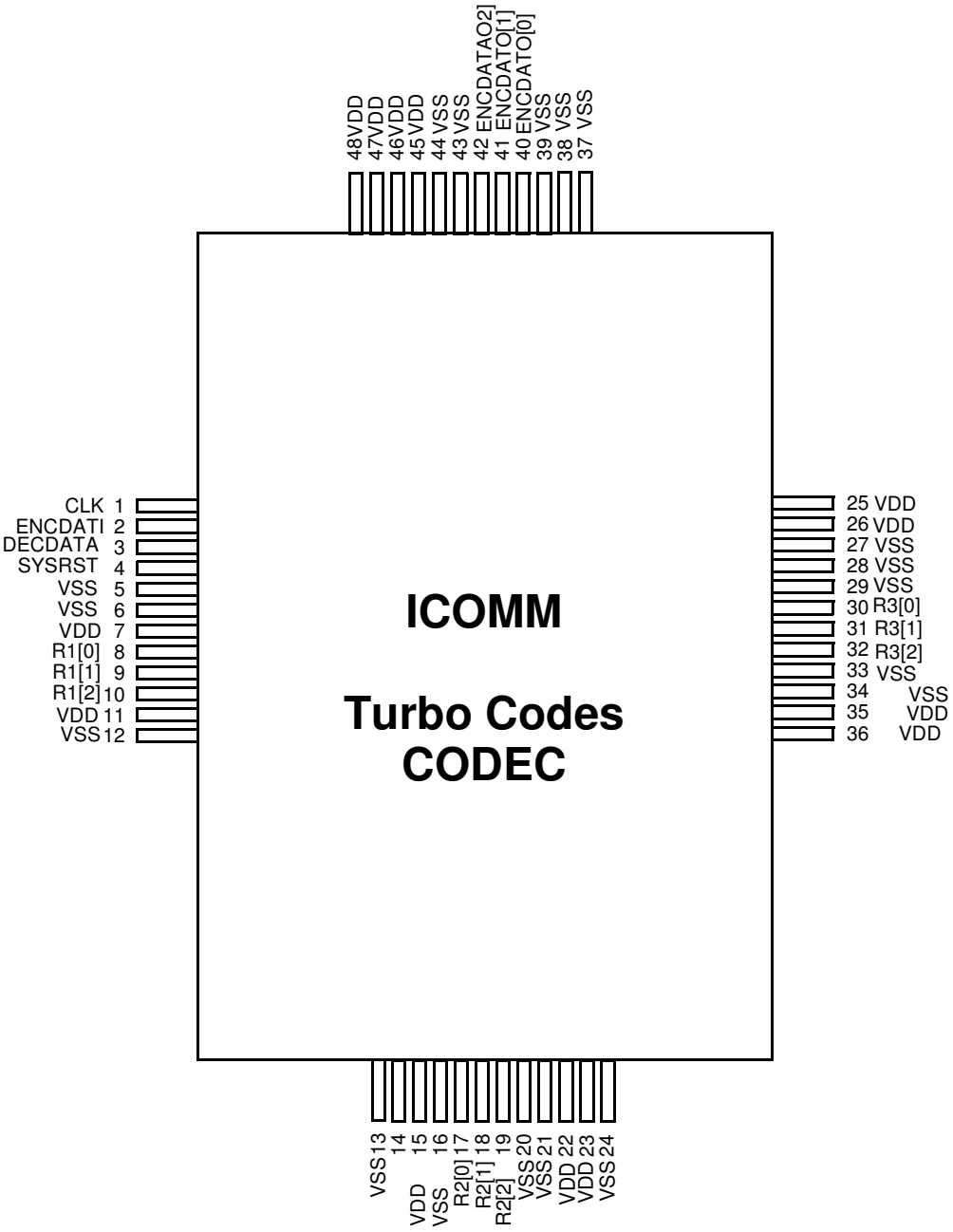


Figure 1. Turbo Codes Codec TQFP Pin Diagram

3 Pin Information (continued)

Functional descriptions of pins 1— 48 are found in Section 6, Signal Descriptions.

Table 1. Turbo Codes Codec Pin Descriptions

TQFP Pin	Symbol	Type	Name/Function
8 - 10	R1[2:0]	I	Soft decision Input R1
17 - 19	R2[2:0]	I	Soft decision Input R2
30 - 32	R3[2:0]	I	Soft decision Input R3
40 - 42	ENCDATO[2:0]	O	Encoded data Output
4-6, 12-14	VSS	P	Ground
1	CLK	I	System CLock (400MHz)
2	ENCDATI	I	Encoding Data Input
3	DECDATO	O	Decoding Data Output
7, 15, 22-23	VDD	P	Power
4	SYSRST	I	System Reset.
16, 20-21, 24	VSS	P	Ground
36, 25-26, 45-48	VDD	P	Power
33-34, 27-29	VSS	P	Ground
37-39, 43-44	VSS	P	Ground

4 Hardware Architecture

4.1 Turbo Codes Encoder

Turbo Codes Encoder employs two (2) Recursive Systematic Convolutional (RSC) Encoder with Coding rate 1/3, Constraint length = 3, connected in parallel with an Interleaver preceding the second RSC encoder.

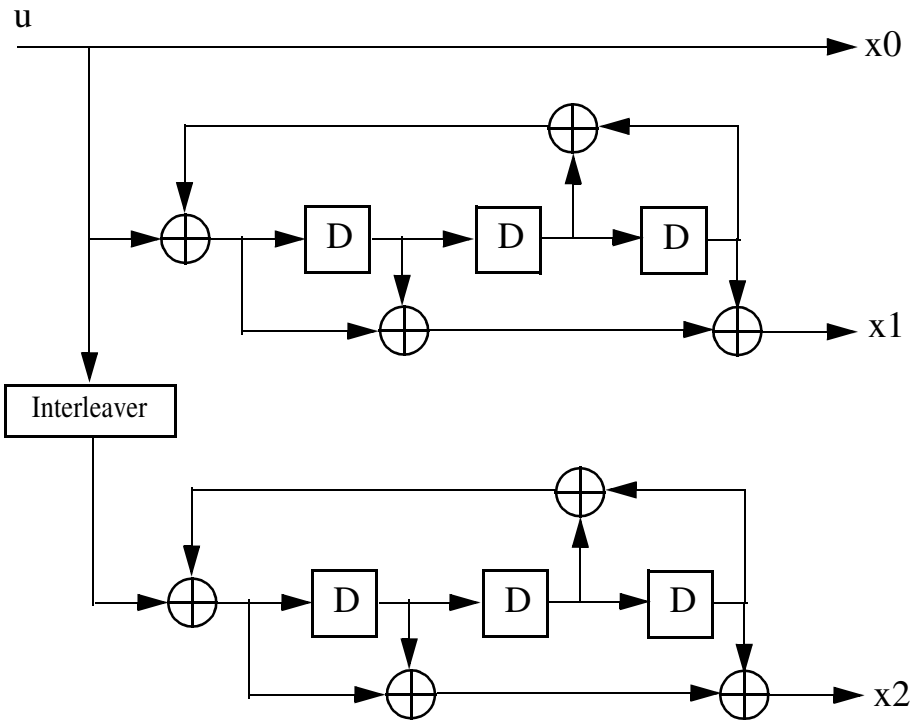


Figure 2. I Parallel Concatenated Convolutional Code (PCCC)

Where:

the transfer function of the 8-state constituent code for PCCC is:

$$G(D) = [1, n(D) / d(D)]$$

where, $d(D) = 1 + D2 + D3$, $n((D) = 1 + D + D3$

4.2 Turbo Codes Decoder

The Turbo Codes Decoder has two concatenated Log-MAP Decoders connected in a feedback loop with Interleaver and De-Interleaver in between. An input Buffer has three buffers of length N for block-decoding. A control logics module (CLSM) consists of various state-machines which in turn control all the operations of the Turbo Codes Decoder. Signals R2, R1, R0 are the output data of the Shift Registers which are the received data input from the external Demodulator. Signal XO1, and XO2 are the output of the Log-MAP Decoders A and B respectively, which are stored in the Interleaver/De-Interleaver modules. Signal Z2 and Z1 are the output of the Interleaver/De-Interleaver which Z2 is feedback into Log-MAP decoder B, and Z1 is feedback into Log-MAP decoder A for iterative decoding.

The Turbo Codes Decoder decodes 8-state Parallel Concatenated Convolutional Code (PCCC), with coding rate 1/3, constraint length K=4, decoding Trellis diagram for Log-MAP (Maximum a Posteriori) Decoder.

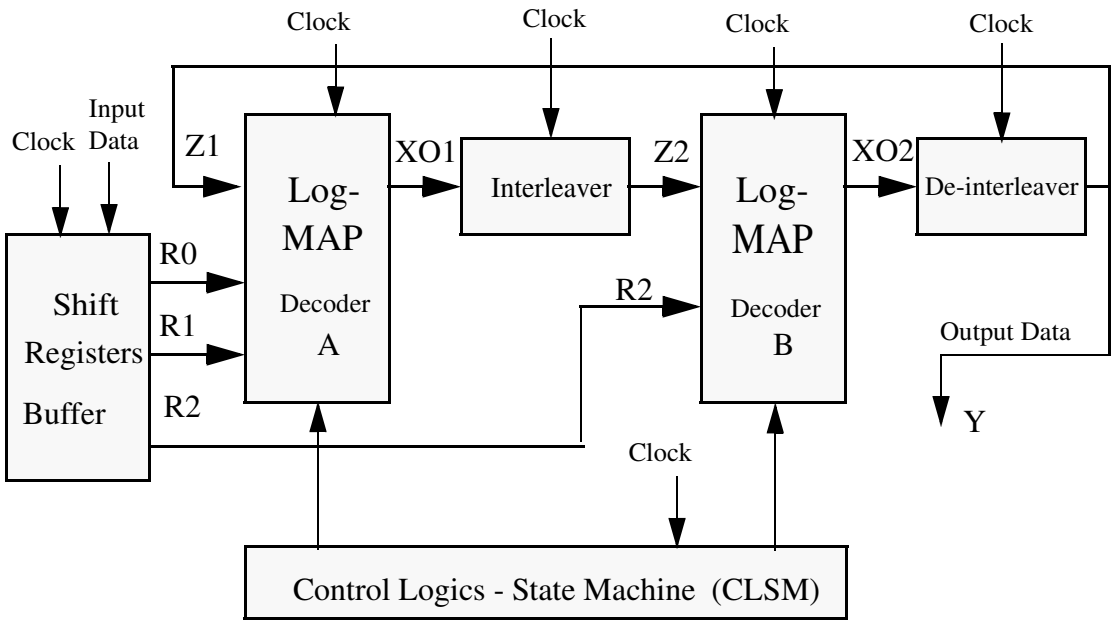


Figure 3. Turbo Codes Decoder Functional block diagram

4.3 Soft Decision Values

Table 2: Soft Decision values input

Soft-Decision Value	Significance
011	Most confident positive value
010	Average confident positive value
001	Least confident positive value
000	no decision
111	Least confident negative value
110	Average confident negative value
101	Most confident negative value

4.4 Log-MAP Decoder block diagram

The Log-MAP Decoder consists of a Branch Metric (BM) computation module, a State Metric (SM) computation module, a Log-MAP computation module, a BM Memory module, a SM Memory module, a Soft-Value Conversion module, and a Control Logic State Machine module. Input data bits enter the Soft-Value Conversion module are assigned 3-bit values according to the TABLE 1. Soft-values inputs then enter the Branch Metric (BM) computation module, where Euclidean distance is calculated for each branch, the output branch metrics are stored in the BM Memory module. The State Metric (SM) computation module reads branch metrics from the BM Memory and compute the state metric for each state, the output state-metrics are stored un the SM Memory module. The Log-MAP computation module reads both branch-metrics and state-metrics from BM memory and SM memory modules to compute the Maximum a Posteriori probability and produce hard-decision output. The Control Logic State-machine module provides the overall operations of the decoding process.

The Turbo Codes Decoder decodes a block of N data bits at a time. Therefore, the Interleaver/De-interleaver length will be N bits, the Shift Registers length will be N bits, the BM and SM Memory modules will be N words. The Turbo Codes Trellis diagram will have N+1 state stages, and N branch stages.

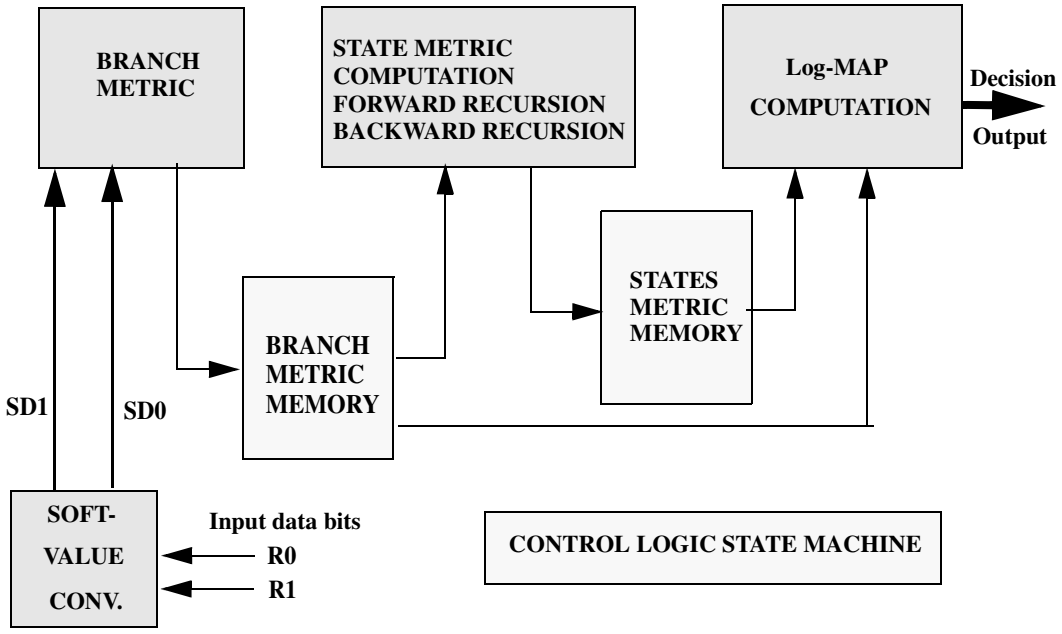


Figure 4. Log-MAP Decoder Functional block diagram

- Branch Metric block computes the Soft-Decision information and produces a set of M branch metrics
- Forward Recursion compute the probabilities of trellis states in forward direction
- Backward Recursion compute the probabilities of trellis states in backward direction
- The Maximum A Posteriori is computed and Soft-Decision output is computed

5 Signal Descriptions

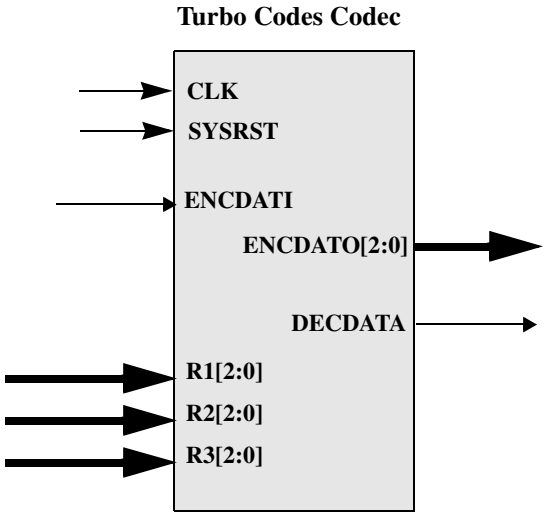


Figure 5. Turbo Codes Codec Signals by Interface

5 Signal Descriptions (continued)

R1[2:0]

Soft Decision data input: 3-bit soft decision data input from the receiver correlator.

R2[2:0]

Soft Decision data input: 3-bit soft decision data input from the receiver correlator.

R3[2:0]

Soft Decision data input: 3-bit soft decision data input from the receiver correlator.

ENCDATO[9:0]

Encoded Data: 3-bit encoded data output from the Turbo Coded Encoder.

DECDATA

Decoded Data: serial decoded data output from the Turbo Codes Decoder.

CLK

System Clock: System clock up to 400MHz.

SYSRST

System Reset: system reset. Positive assertion. A low-to-high transition causes the Turbo Codes Codec processor to enter the reset state.

ENCDATI

Encode data: serial encoding data input

6 Device Characteristics

6.1 Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

External leads can be bonded and soldered safely at temperatures of up to 300 °C.

Voltage Range on Any Pin ..... .V_{SS} – 0.5 V to V_{DDe} + 0.5 V
Power Dissipation ..... 120 mW
Ambient Temperature Range..... 0 °C to +70 °C
Storage Temperature Range.....–65 °C to +150 °C

6.2 Handling Precautions

All MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. Although input protection circuitry has been incorporated into the devices to minimize the effect of this static buildup, proper precautions should be taken to avoid exposure to electrostatic discharge during handling and mounting. IComm Technologies employs a human-body model for ESD susceptibility testing. Since the failure voltage of electronic devices is dependent on the current, voltage, and hence, the resistance and capacitance, it is important that standard values be employed to establish a reference by which to compare test data. Values of 100 pF and 1500 Ω are the most common and are the values used in the IComm Technologies human-body model test circuit. The breakdown voltage for the Turbo Codes Codec is greater than 2000 V.

6.3 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Support Status	Device Speed	Input Clock	Package	Supply Voltage V_{DD} (V)		Ambient Temperature T_A (°C)	
				Min	Max	Min	Max
Today	5 ns	Osc CLock	TQFP	2.7	3.6	0	70

6 Device Characteristics (continued)

Package Thermal Considerations

The recommended operating temperature specified above is based on the maximum power, package type, and maximum junction temperature. The following equations describe the relationship between these parameters. If the applications' maximum power is less than the worst-case value, this relationship determines a higher maximum ambient temperature or the maximum temperature measured at top dead center of the package.

$$T_A = T_J - P \times \Theta_{JA}$$

$$T_{TDC} = T_J - P \times \Theta_{J\text{-}TDC}$$

where T_A is the still-air ambient temperature and T_{TDC} is the temperature measured by a thermocouple at the top dead center of the package.

Maximum Junction Temperature (T_J) in 48-pin TQFP	100 °C
48-pin TQFP Maximum Thermal Resistance in Still-Air-Ambient (Θ_{JA})	40 °C/W
48-pin TQFP Maximum Thermal Resistance, Junction to Top Dead Center ($\Theta_{J\text{-}TDC}$)	40 °C/W

7 Electrical Characteristics and Requirements

The following electrical characteristics are preliminary and are subject to change. Electrical characteristics refer to the behavior of the device under specified conditions. Electrical requirements refer to conditions imposed on the user for proper operation of the device. The parameters below are valid for the conditions described in Section 6.3, Recommended Operating Conditions.

7.1 Input Buffers

Table 4. Electrical Characteristics and Requirements

Parameter	Symbol	Min	Max	Unit
Input Voltage:				
Low	VIL	—	0.3 * VDD	V
High	VIH	0.7 * VDD	—	V
Input Voltage:				
Low	VIL	—	0.8	V
High	VIH	2.0	—	V

8 Electrical Characteristics

Turbo Codes Codec Electrical Characteristics

The following electrical characteristics are preliminary and are subject to change. Electrical characteristics refer to the behavior of the device under specified conditions. Electrical requirements refer to conditions imposed to the user for proper operation of the device.

Table 5. Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Input Voltage:				
Low	V_{IL}	—	0.3 * V_{DD}	V
High	V_{IH}	0.7 * V_{DD}	—	V
Input Current Without Pull-up or Pull-down*:				
High (V_{IH} = 3.6 V, V_{DD} = 3.6 V)	I_{IH}	—	5	µA
High (V_{IH} = ~1.8 V to 3.6 V, V_{DD} = 3.6 V)	I_{IH}	—	20	µA
Low (V_{IL} = 0.0 V, V_{DD} = 3.6 V)	I_{IL}	–5	—	µA
Low (V_{IL} = 0.0 V to ~1.8 V, V_{DD} = 3.6 V)	I_{IL}	–20	—	µA
Input Current with Pull-up:				
High (V_{IH} = 3.6 V, V_{DD} = 3.6 V)	I_{IH}	—	5	µA
Low (V_{IL} = 0.0 V, V_{DD} = 3.6 V	I_{IL}	–40	—	µA
Input Current with Pull-down:				
High (V_{IH} = 3.6 V, V_{DD} = 3.6 V)	I_{IH}	—	40	µA
Low (V_{IL} = 0.0 V, V_{DD} = 3.6 V)	I_{IL}	–5	—	µA
Output Voltage:				
Low:				
(I_{OL} = 2 mA)	V_{OL}	—	0.4	V
(I_{OL} = 50 µA)	V_{OL}	—	0.2	V
High:				
(I_{OH} = –2 mA)	V_{OH}	V_{DD} – 0.7	—	V
(I_{OH} = –50 µA)	V_{OH}	V_{DD} – 0.2	—	V
Output 3-state Current Without Pull-up or Pull-down:				
Low (V_{DD} = 3.6 V, V_{IL} = 0 V)	I_{OZL}	–10	—	µA
High (V_{DD} = 3.6 V, V_{IH} = 3.6 V)	I_{OZH}	—	10	µA

Input Capacitance	C_I	—	5	pF

* Note: this current is due to a "weak-feedback" circuit that latches the state of the input and ioput pins that do not have a pull-up or pull-down (intended to insure floating pins do not remain at the input threshold). The circuit is composed of a weak inverter that drives the value of the input back onto the pin. Hence when pin is above the V_{IH} threshold, it acts as a pull-up and when the pin is below the V_{IL} threshold, it acts as a pull-down. For the case when the pin is in between the V_{IH} high and V_{IL} low thresholds it cannot be determined whether it will pull-up or pull-down.

Table 6. Electrical Characteristics and Requirements

Parameter	Symbol	Min	Max	Unit
Input Voltage:				
Low	V_{IL}	—	0.3 * V_{DDe}	V
High	V_{IH}	0.7 * V_{DDe}	—	V
Input Current without pull-up or pull-down:				
Low (V_{IL} = 0 V, V_{DDe} = 3.6 V)	I_{IL}	–5	—	µA
High (V_{IH} = 5.25 V, V_{DDe} = 3.6 V)	I_{IH}	—	5	µA
Input Current with pull-up:				
Low (V_{IL} = 0 V, V_{DDe} = 3.6 V)	I_{IL}	–30	—	µA
High (V_{IH} = 3.6 V, V_{DDe} = 3.6 V)	I_{IH}	—	5	µA
Input Current with pull-down:				
Low (V_{IL} = 0 V, V_{DDe} = 3.6 V)	I_{IL}	-5	—	µA
High (V_{IH} = 3.6 V, V_{DDe} = 3.6 V)	I_{IH}	—	30	µA
Output Low Voltage:				
Low (I_{OL} = 2.0 mA)	V_{OL}	—	0.4	V
Low (I_{OL} = 50 µA)	V_{OL}	—	0.2	V
Output High Voltage:				
High (I_{OH} = –2.0 mA)	V_{OH}	V_{DDe} – 0.7	—	V
High (I_{OH} = –50 µA)	V_{OH}	V_{DDe} – 0.2	—	V
Output 3-State Current without pull-up or pull-down:				
Low (V_{DDe} = 3.6 V, V_{IL} = 0 V)	I_{OZL}	–10	—	µA
High (V_{DDe} = 3.6 V, V_{IH} = 5.25 V)	I_{OZH}	—	10	µA
Input Capacitance	C_I	—	5	pF
Frequency of Ring Oscillator (selected with SLOWCLK)	F_{RO}	2.5	0.5	MHz

Table 7. Electrical Requirements for Input Clock Oscillator

Parameter	Symbol	Min	Max	Unit
CMOS Level Input Voltage:				
Low	V_{IL}	—	0.3 * V_{DDe}	V
High	V_{IH}	0.7 * V_{DDe}	—	V

8 Electrical Characteristics and Requirements (continued)

8.1 Power Dissipation

The typical power dissipation listed is for a selected application. The following electrical characteristics are preliminary and are subject to change.

Table 8. Power Dissipation (not including pin activity)

Parameter	Symbol	Typical	Units
Active Power Dissipation: Clock @ 200 MHz	$PD_{DACTIVE}$	10	mw
Idle Power Dissipation: Clock @ 200 MHz	PD_{IDLE}	2	mw
Sleep Power Dissipation: Clock @ 200 MHz	PD_{SLEEP}	1.5	mw
Power-Down Power Dissipation: Clock Disabled	PD_{PWRDWN}	0.6	mw

The power dissipation listed is for internal power dissipation only. Total power dissipation can be calculated on the basis of the application by adding C x V_{DD}^2 x f for each output, where C is the additional load capacitance and f is the output frequency.

Power dissipation due to the input buffers is highly dependent on the input voltage level. At full CMOS levels, essentially no dc current is drawn. However, for levels between the power supply rails, especially at or near the threshold of $V_{DD}/2$, high currents can flow. Although input and I/O buffers may be left untied, it is still recommended that unused input and I/O pins be tied to V_{SS} or V_{DD} through a 10 kΩ resistor to avoid application ambiguities. Further, if I/O pins are tied high or low, they should be pulled fully to V_{SS} or V_{DD}.

Electrical Characteristics and Requirements (continued)

Table 9. Power Dissipation of Individual Sections

Parameter	Symbol	Typical	Units
Turbo Codes Codec Power Dissipation	PD	0.050	mw / MHz

The total power dissipation of the Turbo Codes Codec is:

$PDTOTAL = PD + PDOUTPUTS$

$PDOUTPUTS = COUTPUT \times VDD^2 \times FOUTPUT$

Power dissipation due to the input and I/O buffers is highly dependent on the input voltage level. At full CMOS levels, essentially no dc current is drawn. However, for levels near the threshold of $0.5 \times VDD$, high and unstable levels can flow. Therefore, all unused input pins should be tied inactive to VDD or VSS, and all unused I/O pins should be tied inactive through a 10 kΩ resistor to VDD or VSS.

9 Timing Characteristics

The following timing characteristics and requirements are preliminary information and are subject to change. Timing characteristics refer to the behavior of the device under specified conditions. Timing requirements refer to conditions imposed on the user for proper operation of the device. All timing data is valid for the following conditions:

T_A = 0 °C to +70 °C (See Section 6.3.)

V_{DD} = 5 V ± 5%, V_{SS} = 0 V (See Section 6.3.)

Capacitance load on outputs (C_L) = 50 pF

Output characteristics can be derated as a function of load capacitance (C_L).

All outputs: 0.03 ns/pF ≤ dt/dC_L ≤ 0.06 ns/pF for 10 ≤ C_L ≤ 100 pF

at V_{IH} for rising edge and at V_{IL} for falling edge

For example, if the actual load capacitance is 30 pF instead of 50 pF, the derating for a rising edge is

(30 – 50) pF x 0.06 ns/pF = 1.2 ns **less** than the specified rise time or delay that includes a rise time.

Test conditions for inputs:

- Rise and fall times of 4 ns or less
- Timing reference levels for delays = V_{IH}, V_{IL}

Test conditions for outputs (unless noted otherwise):

- C_{LOAD} = 50 pF;
- Timing reference levels for delays = V_{IH}, V_{IL}
- 3-state delays measured to the high-impedance state of the output driver

9 Timing Characteristics (continued)

9.1 Turbo Codes Codec System Clocks

The maximum speed of the Turbo Codes Codec has been increased to 400MHz (5ns).

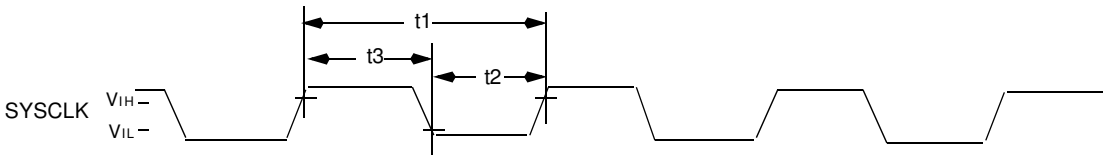


Figure 6. System Clock Timing Diagram

Table 10. Timing Requirements for Input Clock

Abbreviated Reference	Parameter	Min	Max	Unit
t1	Clock In Period (high to high)	2.5	—†	ns
t2	Clock In Low Time (low to high)	1.25	—	ns
t3	Clock In High Time (high to low)	1.25	—	ns

9 Timing Characteristics (continued)

9.2 Turbo Codes Codec Data I/O Specifications

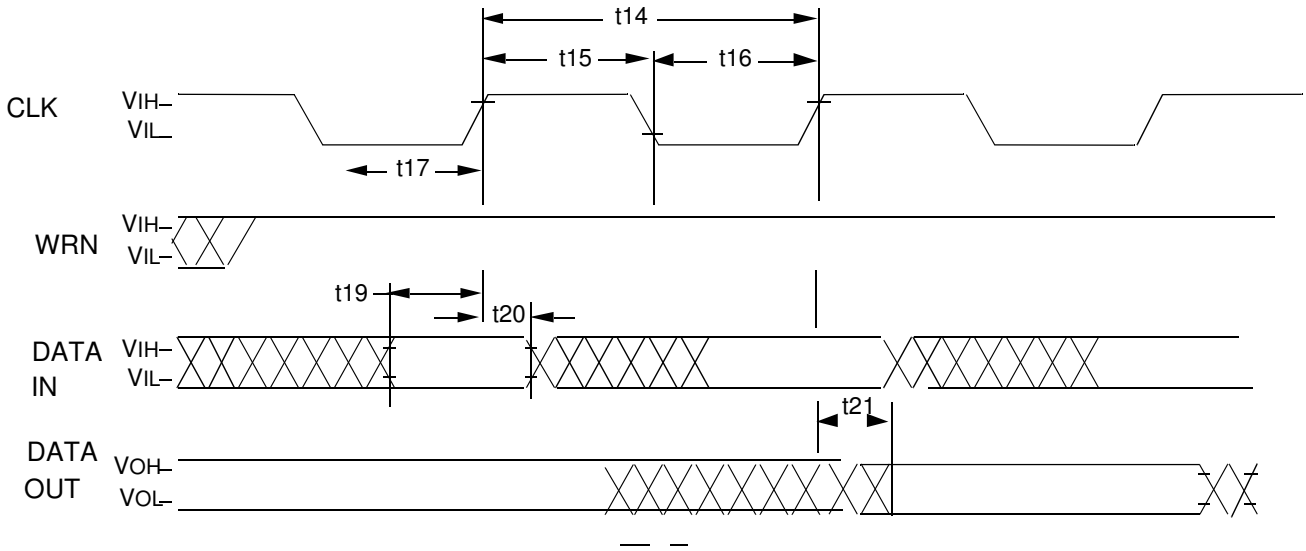


Figure 7. Turbo Codes Codec Data I/O Timing Diagram

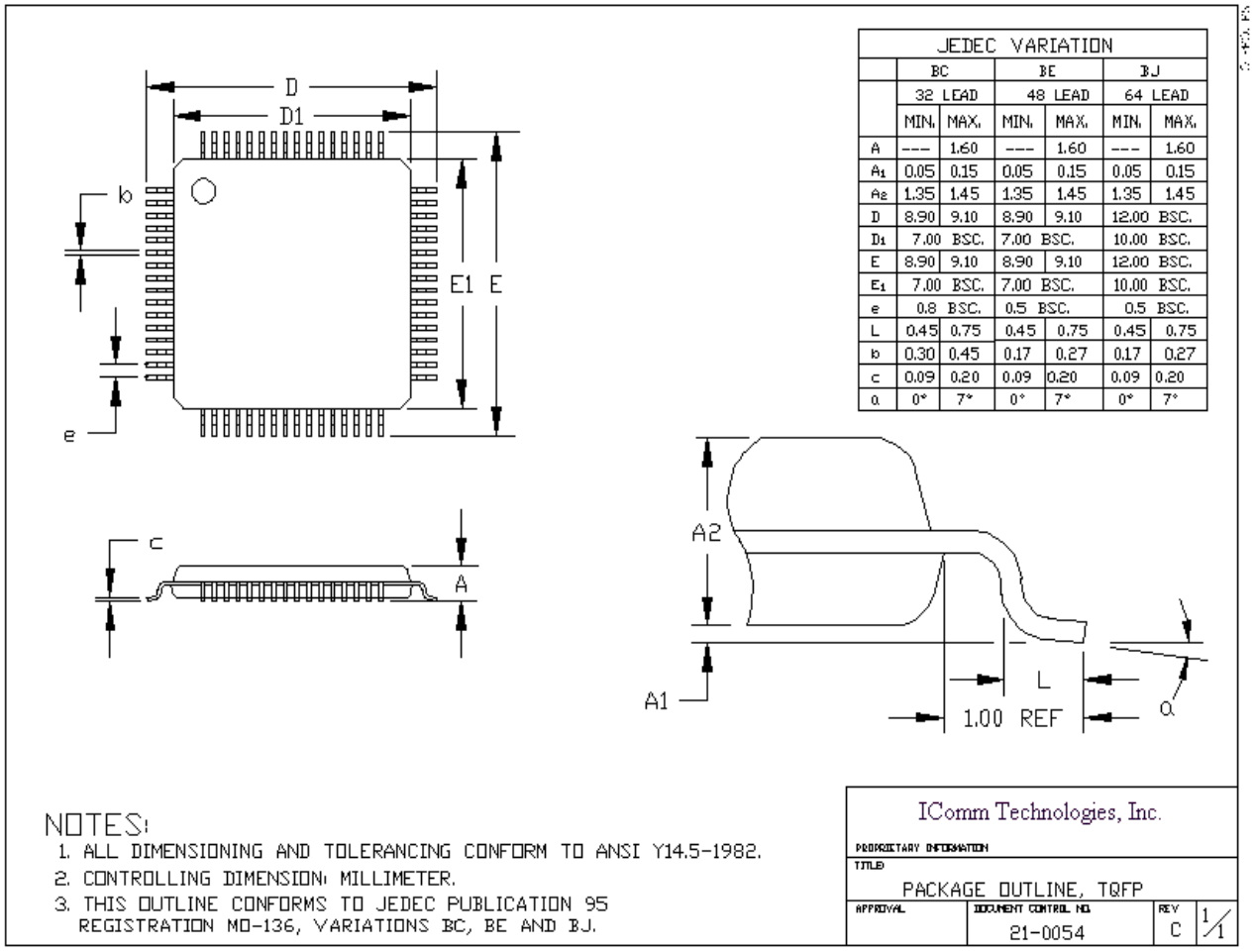
Table 11. Timing Requirements for Turbo Codes Codec I/O

Abbreviated Reference	Parameter	Min	Max	Unit
t14	CLK Period (high to high)	2.5	—	ns
t15	CLK High Time (high to low)	1.25	—	ns
t16	CLK Low Time (low to high)	1.25	—	ns
t21	Dat Out Delay (high to valid)	—	5	ns
t19	Data Input Setup Time (valid to high)	.5	—	ns
t20	Data Input Hold Time (high to invalid)	.5	—	ns

10 Outline Diagrams

10.1 48-pin TQFP (Thin Quad Flat Pack)

All dimensions are in millimeters.



JEDEC VARIATION						
	BC		BE		BJ	
	32 LEAD		48 LEAD		64 LEAD	
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
A	---	1.60	---	1.60	---	1.60
A_1	0.05	0.15	0.05	0.15	0.05	0.15
A_2	1.35	1.45	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10	12.00 BSC.	
D_1	7.00 BSC.		7.00 BSC.		10.00 BSC.	
E	8.90	9.10	8.90	9.10	12.00 BSC.	
E_1	7.00 BSC.		7.00 BSC.		10.00 BSC.	
e	0.8 BSC.		0.5 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27	0.17	0.27
c	0.09	0.20	0.09	0.20	0.09	0.20
θ	0°	7°	0°	7°	0°	7°

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS BC, BE AND BJ.

IComm Technologies, Inc.		
PROPRIETARY INFORMATION		
TITLE: PACKAGE OUTLINE, TQFP		
APPROVAL	DOCUMENT CONTROL NO. 21-0054	REV C
		1/1